Remarks

Thorough examination by the Examiner is noted and appreciated.

The Specification has been amended to correct grammatical errors including as noted by Examiner.

The claims have been amended to clarify Applicants invention to define over the prior art.

No new matter has been added.

For example, support for the amendments is found in the originally presented claims, the Figures (Figures 5 and 6), and the Specification(shown as previously amended):

[0040] The configuration illustrated in FIG. 6 enables ECC circuit 70 **to correct the correctable error when accessing repairing formation from information array 52**. The repairing information can be obtained correctly even if a corrupted bit is present. This configuration thus improves the repairing efficiency **when the information array 52 shares the same read/write circuit** and bit lines **with main array 50**. If an ECC circuit, such as ECC circuit 70, is not available, corrupted bits in information array 52 will render the chip unrepairable.

[0041] FIG. 6 thus depicts a configuration that may be utilized to improve column and/or row repairing efficiency in non-volatile memory devices, such as, for example, EPROM, EEPROM and Flash

memory devices. Column and/or row repairing data may be read from information array 52, which is associated with the non-volatile memory and can form part of main array 50. This repairing data is generally read to volatile latches (e.g., volatile latch array 60) associated with the non-volatile memory. **ECC circuit 70 can be enabled during reading of the repairing data for identifying and repairing defective rows and/or columns associated with the non-volatile memory, despite an error in the repairing information caused by a defective column.** ECC circuit 70 can thus be enabled during an access of main array 50 (i.e., which is associated with the non-volatile memory) to thereby correct a correctable error if a particular address corresponds to an address of at least one defective row and/or column. This particular address may, for example, comprise a Y-address corresponding to a defective column.

[0039] An error correction coding (ECC) circuit 70 is linked to volatile latch array 60, which in turn is connected to decoder circuit 62. ECC circuit 70 can be enabled through ECC enabling circuit 72, which is connected to ECC circuit 70. Read circuit 58 can access main memory 50 and transfer data to ECC circuit 70. To achieve improved row and column repair, information may be read from information array 52 to volatile latch array 60 after system power-up. During access of main array 50, ECC circuit 70 is enabled to correct correctable errors if a Y-address corresponds to an address indicative of a corrupt or defective row and/or column. **During the read-out of repairing information from information array 52, ECC circuit 70 is always enabled to repair any correctable errors of data. The correct repairing information can be read out of information array 52 even if some of the selected columns are defective or corrupted during access of information array 52.**

Claim Rejections 35 USC § 112

Examiner refers to the objection to the drawings to explain a rejection of claim 1-23 based on the written description requirement. Examiner has also objected to the drawings on the

basis that the drawings must show every feature of the invention specified in the claims.

"Therefore, the "respective I/O terminal" associated with "each of said plurality of columns" where the "columns" "are associated with said non-volatile memory" must be shown or the features canceled from the claims. The drawings filed 14 September 2005 to not show any columns and it is not supposed that there is a one-to-one correspondence with the terminals (16) shown and the "columns" of the non-volatile memory (14).

Examiner has further stated that:

"Judging by the amendments to the drawings and specification, the claimed association between nonvolatile memory array columns and "respective I/O terminal" is a conventional selective coupling arrangement for accessing columns of nonvolatile memory arrays and is met by Mangan. Unless applicants objects in response to this interpretation, the objection to the drawing and the corresponding rejection of the claims under 35 USC 112, 1st paragraph, will not be maintained in the next Office action.

Applicants do not dispute that association of a memory array column with an I/O terminal may be conventional as stated in the Specification: The (16,11) Hamming code is well known in the are and is described as pg. 64 of "Error control Coding; Fundamentals and Applications," by Shu Lin & Daniel J. Costello, Jr.).

However, Applicants do not agree that Mangan discloses Applicants invention.

It is further noted that Applicants are not required to show what is conventional in the drawings including rows and columns which conventionally form arrays.

With respect to the written description requirement, Examiner is referred to the MPEP:

> **ADEQUACY OF WRITTEN DESCRIPTION**
> ***A. Read and Analyze the Specification for Compliance with 35 U.S.C. 112, para. 1***
> Office personnel should adhere to the following procedures when reviewing patent applications for compliance with the written description requirement of 35 U.S.C. 112, para. 1. **The examiner has the initial burden, after a thorough reading and evaluation of the content of the application, of presenting evidence or reasons why a person skilled in the art would not recognize that the written description of the invention provides support for the claims.** There is a strong presumption

that an adequate written description of the claimed invention is present in the specification as filed, *Wertheim*, 541 F.2d at 262, 191 USPQ; however, with respect to newly added or claims, applicant should show support in the disclosure for the new or amended claims.

"[I]n considering the disclosure of a reference, it is proper to take into account not only specific teachings of the reference but also the inferences which one skilled in the art would reasonably be expected to draw therefrom." *In re Preda*, 401 F.2d 825, 826, 159 USPQ 342, 344 (CCPA 1968)

It is now well accepted that a satisfactory description may be in the claims or any other portion of the originally filed specification.

See MPEP, 8th Ed, Section 2163 (I)

While there is **no *in haec verba* requirement,** newly added claim limitations must be supported in the specification through **express, implicit, or inherent disclosure.**

See MPEP, 8th Ed, Section 2163 (I) (B)

The fundamental factual inquiry is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. See, e.g., *Vas-Cath, Inc.*, 935 F.2d at 1563-64, 19 USPQ2d at 1117.

Possession may be shown in many ways. For example, possession may be shown **by describing an actual reduction to practice of the claimed invention.** Possession may also be shown by a clear depiction of the invention in detailed drawings or in structural chemical

> formulas which permit a person skilled in the art to clearly recognize that applicant had possession of the claimed invention. **An adequate written description of the invention may be shown by any description of sufficient, relevant, identifying characteristics so long as a person skilled in the art would recognize that the inventor had possession of the claimed invention.** See, e.g., *Purdue Pharma L.P. v. Faulding Inc.*, 230 F.3d 1320, 1323, 56 USPQ2d 1481, 1483 (Fed. Cir. 2000).

Applicants respectfully contend that Examiner has not made out a prima facie case that Applicants claim language violates the written description requirement.

Claim Rejections 35 USC § 103

1. Claims 1-20, 22 and 23 stand rejected under 35 U.S.C. §103 (a) as being unpatentable over Mangan et al. (US 5,471,478).

Mangan et al. disclose a file structure employed in a flash EEPROM system where an array of rows and columns are divided into cells that are separately addressable for the purpose of erasing an entire block of cells at the same time. **Columns** of cells are used as spare cells to replace defective

cells and **store overhead (header) information** including pointers to locations of defective sector data cells as well as **error correction codes** for the sector data and the header information (see Abstract).

The invention of Mangan et al. provides a few spare cells as part of the header with pointers to bad cell addresses which are then replaced with the spare cells (col 2, lines 37-46). **In order to overcome the problem that the header information may be located in areas that have bad cells,** the method of Mangan et al. **improves the probability** that the header information will be located **in areas that do not have bad cells** by providing **two separately positioned header portions** (columns) (positioned in narrow stacks 215 and 217; Figure 4)(col 2, lines 40-47; col 5, lines 40-48) "**in order to be assured that at least critical portions of the stacks are formed where there are not defective EEPROM cells**". Error correction codes (ECC) as well as spare data bits for bit/column replacement are also provided in the separately positioned stack header portions e.g., 217 (see Figure 5; col 5, lines 49-64).

One of he header stacks 215 **has the ability to operate with a few bad cells** (col 6, lines 9-21; Fig 6) by bit remapping

(creating bad bit pointers). The bad bit pointers are loading during a testing procedure (col 6, lines 23-24) to map bad cells out of the system **however, row 0** of stack 215 **must be located in an area where not defective cells exist.** "This is made possible because of the ability to move the stacks 215 and 217 from left to right by appropriately noting their chunk column addresses in the controller 133" (see (col 6, lines 28-30). **An error correction code ECC is calculated from information in row 0** (col 6, lines 34-40).

Thus, the method and memory structure of Mangan et al. creates the very problem that Applicants invention solves and fails to disclose the following elements of Applicants invention including those elements in **bold type:**

With respect to claim 1:

"A method for improving repairing efficiency in a non-volatile memory, said method comprising the steps of:

reading repairing data from an information array associated with said non-volatile memory to a **volatile latch array** associated with said non-volatile memory, **said information array sharing a read circuit with a main memory array comprising said**

non-volatile memory; and,

enabling an error correction coding circuit **separate from said information array** during reading of said repairing data **including corrupted repairing data located anywhere in said information array, said repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read."**

With respect to claim 11:

" A system for improving repairing efficiency in a non-volatile memory, said system comprising:

a reading circuit for reading repairing data from an information array associated with said non-volatile memory to a **volatile latch array** associated with said non-volatile memory, **said information array sharing said read circuit with a main memory array comprising said non-volatile memory;** and,

an error correction coding circuit separate from said information array **adapted to be enabled during reading of said repairing data including reading corrupted repairing data**

located anywhere in said information array, said **repairing data for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read."**

Thus, in the memory structure and method of Magan, at least one of the rows (i.e., row 0) of one of the columns or stacks including repair data (header information) and including error correction codes must be in good cells or be non-corrupted, thus disclosing a different principle of operation than Applicants method where an error correction coding circuit separate from said information array is enabled "during reading of said repairing data **including reading corrupted repairing data located anywhere in said information array" "for identifying and repairing defective columns or rows comprising said main memory array despite corruption of the repairing data as read."**

Moreover, any modification of Magan et al. in an attempt to reproduce Applicants invention would change the **principle of operation (of having at least row 0 of a header stack including repair information such as error correction codes being non-corrupted)** of the method and system of Magan et al. and make the method and system of Magan et al. **unsuitable for its intended**

purpose (of having at least row 0 of a header stack including repair information such as error correction codes being non-corrupted).

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

"**First**, there must be some **suggestion or motivation**, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. **Second**, there must be a **reasonable expectation of success**. **Finally**, the prior art

reference (or references when combined) **must teach or suggest all the claim limitations**. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)*.

Conclusion

The cited reference fails to disclose or suggest Applicants invention and is therefore insufficient to make out a *prima facie* case of obviousness.

Applicants have amended their claims to further clarify their invention and to clearly define over the cited art. Applicants respectfully request favorable consideration of their claims.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

In the event that the present invention as claimed is not in

condition for allowance for any reason, the Examiner is respectfully invited to call the Applicants= representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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